REMARKS

This is a full and timely response to the Office Action of August 10, 2004. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this Third Response, claims 1-30 are pending in this application. Claims 1, 3, 4, 7, 12, 20, 21, and 30 have been directly amended herein. It is believed that the foregoing amendments add no new matter to the present application.

Response to §103 Rejections

"The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted). Furthermore, "(o)ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine,* 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Claim 1 reads as follows:

> 1. A computer system for efficiently executing instructions of computer programs, comprising:
>
> processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;
>
> cache memory;
>
> computer memory having a plurality of addresses; and
>
> memory control circuitry coupled to said processing circuitry, said ***memory control circuitry configured to store, in response to said first context switch command, in computer memory data written by said pipeline during execution of said one program and to store an indicator indicative of how often a portion of said cache memory is accessed in executing said instructions from said one program***, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing said indicator corresponding to data previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, said memory control circuitry further configured to retrieve said data from said computer memory in response to said second context switch command and to store said retrieved data in said cache memory based upon said indicator. (Emphasis added).

Applicants respectfully assert that the alleged combination of *Novak* and *Gulsen* fails to teach or suggest at least the features of claim 1 highlighted hereinabove.

In this regard, the Office Action states:

> "Novak has taught identifying data previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, but has not explicitly taught how to handle when the second task must overwrite data for the first task in shared resources."

Further, it appears that Gulsen teaches a system that stores data associated with a particular task in "backing store" based upon a calculation of shared resources needed by an incoming task. However, neither Novak or Gulsen teaches "memory

control circuitry configured to store, in response to said first context switch command, in computer memory data written by said pipeline during execution of said one program and to store an indicator indicative of how often a portion of said cache memory is accessed in executing said instructions from said one program," as claimed in claim 1.

Thus, Applicant respectfully submits that the combination of *Novak* and *Gulsen* does not teach or suggest those limitations highlighted in amended claim 1. Accordingly, for at least the reasons set forth above, Applicant respectfully submits that the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

Claims 2-6, 28, 29

Claims 2-6, 28, and 29 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 2-6, 28, and 29 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2-6, 28, and 29 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Claim 7 reads as follows:

7. A computer system for efficiently executing instructions of computer programs, comprising:

processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;

cache memory;

computer memory having a plurality of addresses; and

memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to maintain a plurality of mappings, said mappings respectively correlating data values previously written by said pipeline during execution of an instruction and stored in said cache memory with said memory addresses of said computer memory, ***said memory control circuitry configured to store in said computer memory said mappings and information indicating whether said cache memory corresponding to said mappings was recently accessed in response to said first context switch command and to retrieve said data values from said addresses that are identified by said mappings stored in said computer memory in response to said second context switch command based upon said information,*** said memory control circuitry further configured to store in said cache memory said retrieved data values. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach at least those limitation highlighted hereinabove. Accordingly, Applicant requests that the 35 U.S.C. §103 rejection of claim 7 be withdrawn.

Claims 8-11

Claims 8 through 11 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 8 through 11 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8 through 11 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or

combinations of features that make them allowable, notwithstanding the allowability of their base claim 7.

Claim 12

Claim 12 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Claim 12 reads as follows:

> 12. A method for efficiently executing instructions of computer programs, comprising the steps of:
> executing a plurality of computer programs in an interleaved fashion;
> switching which of said computer programs is being executed in said executing step;
> ***storing, prior to said switching step, at an address in computer memory a data value previously written by a pipeline to cache line in execution of an instruction corresponding to one of said computer programs in said executing step and information indicative of how often said cache line is accessed during execution;***
> identifying said address in response to said switching step;
> ***retrieving said data value from said address based on said identifying step and in response to said switching step based upon said information indicative of how often said cache memory is accessed;***
> storing said retrieved data value in cache memory; and
> retrieving said data value from said cache memory in response to said executing step. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach or suggest the highlighted features of claim 12 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

Claims 13-15

Claims 13 through 15 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 13 through 15 contain all features of their respective independent claim 12. Since claim 12 should be allowed, as argued hereinabove, pending dependent claims 13 through 15 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 12.

Claim 16

Claim 16 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Claim 16 reads as follows:

> 16. A method for efficiently executing instructions of computer programs, comprising the steps of:
> executing instructions from a computer program;
> halting said executing step during a first context switch in response to a first context switch command;
> resuming said executing step during a second context switch in response to a second context switch command;
> maintaining a plurality of mappings;
> ***correlating, via said mappings, data values previously written by a pipeline during the executing step and stored in a cache memory with memory addresses of computer memory outside of said cache memory;***
> ***storing said mappings in said computer memory in response to said first context switch command and information indicative of whether said cache memory storing said data values was accessed during a particular time period;***
> ***retrieving, based on said mappings and said information and in response to said second context switch command, at least one data value from at least one of said addresses identified by said mappings; and***
> storing said at least one retrieved data value in said cache memory. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach or suggest the highlighted features of claim 16 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

Claims 17-19

Claims 17 through 19 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 17 through 19 contain all features of their respective independent claim 16. Since claim 16 should be allowed, as argued hereinabove, pending dependent claims 17 through 19 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 16.

Claim 20

Claim 20 presently stands rejected under 35 U.S.C. §103 as allegedly unpatentable over *Novak* in view of *Gulsen*. Claim 20 reads as follows:

> 20. A computer system for efficiently executing instructions of computer programs, comprising:
> computer memory; and
> a processing unit comprising cache memory and logic configured to store in said computer memory a value indicative of whether a portion of said cache memory was recently accessed by said processor and a mapping associated with said value, said mapping indicative of a location in said computer memory storing data previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process, the logic further configured to

retrieve said data, based on said value, and store said data in said cache, said processing unit continuing execution of said first process with the retrieved data when the processing unit context switches out the second process and context switches in the first process. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach or suggest the highlighted features of claim 20 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

Claims 22-24

Claims 22-24 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 22-24 contain all features of their respective independent claim 20. Since claim 20 should be allowed, as argued hereinabove, pending dependent claims 22-24 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 20.

Claim 21

Claim 21 presently stands rejected under 35 U.S.C., §103 as allegedly unpatentable over *Novak* in view of *Gulsen*. Claim21 reads as follows:

> 21. A method for efficiently executing instructions of computer programs, comprising the steps of:
> storing in memory outside of a processing unit a value indicative of how often cache memory is accessed by said processor;
> ***storing in said memory a mapping corresponding to said value, said mapping indicative of a location in computer memory storing data previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process;***
> ***retrieving said data, based upon said value, when the processing unit context switches out the second process and context switches in the first process;*** and
> continuing execution of said first process with the data retrieved in the retrieving step. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach or suggest the highlighted features of claim 21 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

Claims 25-27

Claims 25-27 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Novak* in view of *Gulsen*. Applicant submits that the pending dependent claims 25-27 contain all features of their respective independent claim 21. Since claim 21 should be allowed, as argued hereinabove, pending dependent claims 25-27 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 21.

Claim 30

Claim 30 presently stands rejected under 35 U.S.C., §103 as allegedly unpatentable over *Novak* in view of *Gulsen*. Claim 30 reads as follows:

> 30. A system, comprising:
> computer memory; and
> a processing unit comprising cache memory, said cache memory comprising a cache line storing data written or read by a first process during execution by said processing unit, said processing unit further comprising logic configured to track an usage frequency of said cache line, ***said logic further configured to store in said computer memory a value indicative of whether the cache line was accessed and to store in memory a mapping associated with said data used from said cache line by said first process upon a first context switch***, said logic further configured to preload said data into said cache upon a second context switch based on said information. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Novak* and *Gulsen* does not teach or suggest the highlighted features of claim 30hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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